WHAT IS CLAIMED:

1. A system comprising:

a master control processor;

a bus controller connected to the master control processor and implementing a serial bus interface between the master control processor and a plurality of serial bus devices, the master control processor and the bus controller being on a first circuit board;

a midplane connected to the bus controller on the first circuit board; and

a plurality of additional circuit boards connected to the serial bus interface through the midplane, each of the plurality of additional circuit boards including

one or more of the serial bus devices,

a switch configured to electrically connect the circuit board corresponding to the switch to the first circuit board through the serial bus interface when the switch is controlled to be in a first state and to electrically isolate the circuit board corresponding to the switch from the serial bus interface on the first circuit board when the switch is controlled to be in a second state, and

local control logic for outputting a signal for controlling the state of the switch, the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state.

2. The system of claim 1, wherein the first circuit board further comprises:

a master control logic circuit connected to the master control processor, the master control logic circuit communicating with the local control logic of each of the additional circuit boards over the midplane.

3. The system of claim 2, wherein the first circuit board further comprises:

a multiplexer connected to the output of the bus controller and dividing the serial bus interface implemented by the bus controller into a plurality of sub-buses, only one of the sub-buses being connected to the bus controller by the multiplexer at any given time.

4. The system of claim 3, wherein the serial bus devices include at least one of a temperature sensor, a voltage monitor, and an ID EPROM.

5. The system of claim 3, wherein one of the serial bus devices includes an ID EPROM connected to the midplane.

6. The system of claim 3, wherein one of the sub-buses is connected to the plurality of additional circuit boards .

7. The system of claim 1, wherein each of the plurality of additional circuit boards includes:

a first switch for selectively connecting or disconnecting a first portion of a serial bus, implemented by the serial bus interface from the first circuit board, to a second portion of the serial bus;

a second switch for selectively connecting or disconnecting the second portion of the serial bus to a third portion of the serial bus; and

a third switch for selectively connecting or disconnecting the third portion of the serial bus to a fourth portion of the serial bus.

8. The system of claim 7, wherein each of the plurality of additional circuit boards further includes:

a local processor; and

a bus controller interfacing the local processor to the fourth portion of the serial bus;

the local control logic circuit being connected to receive control information from the first circuit board and the local processor and control the first, second, and third switches based on the received control information.

9. A network device in a computer network comprising:

a routing engine for consolidating routing information learned from routing protocols in the network; and

a packet forwarding engine connected to the routing engine, the packet forwarding engine including

a midplane;

a first circuit board having a master control processor; and

a plurality of second circuit boards each having a control processor, the first and second circuit boards being electrically coupled through the midplane via a serial control bus, the second circuit boards each additionally including a switch configured to electrically connect the second circuit board to the first circuit board via the serial control bus when the switch is controlled to be in a first state and to electrically isolate the second circuit board from the serial control bus when the switch is controlled to be in a second state, the switch of a particular one of the second circuit boards being in the first state only when the switches on each of the other of the second circuit boards are in the second state.

10. The network device of claim 9, wherein the network device is a network router.

11. The network device of claim 9, wherein the plurality of second circuit boards each additionally comprises:

local control logic connected to receive control information from the master control processor and the control processor corresponding to the second circuit board of the local control logic, the local control logic controlling the switch to be in the first or second state based on the received control information.

12. The network device of claim 11, wherein the first circuit board further comprises:

a master control logic circuit connected to the master control processor, the master control logic circuit communicating with the local control logic of each of the second circuit boards over the midplane.

13. The network device of claim 9, wherein the first circuit board further comprises:

a bus controller connected to the master control processor and implementing an interface for the serial bus.

14. The network device of claim 13, wherein the first circuit board further comprises:

a multiplexer connected to the output of the bus controller and dividing the serial bus interface implemented by the bus controller into a plurality of sub-buses, only one of the sub-buses being connected to the bus controller by the multiplexer at any given time.

15. The network device of claim 14, wherein one of the sub-buses includes, as a bus device, at least one of a temperature sensor, a voltage monitor, and an ID EPROM.

16. The network device of claim 14, wherein one of the sub-buses includes, as a bus device, an ID EPROM connected to the midplane.

17. The network device of claim 14, wherein one of the sub-buses is connected to the plurality of second circuit boards.

18. A circuit board comprising:

a first switch for selectively connecting or disconnecting a first portion of a two wire serial bus from an external circuit board to a second portion of the two wire serial bus;

a second switch for selectively connecting or disconnecting the second portion of the two wire serial bus to a third portion of the two wire serial bus;

a third switch for selectively connecting or disconnecting the third portion of the two wire serial bus to a fourth portion of the two wire serial bus;

a local processor;

a bus controller interfacing the local processor to the fourth portion of the two wire serial bus; and

a local control logic circuit connected to receive control information from the external circuit board and the local processor and control the first, second, and third switches based on the received control information.

19. The circuit board of claim 18, wherein the local control logic circuit operates to connect the external circuit board and the local processor to different portions of the two wire serial bus.

20. The circuit board of claim 18, wherein the local control logic circuit controls the first, second, and third switches so that if the first and second switches are connected, the third switch is disconnected.

21. The circuit board of claim 18, wherein the local control logic circuit controls the first, second, and third switches so that if the first switch is connected and the second switch is disconnected, the third switch is connected.

22. The circuit board of claim 18, wherein the local control logic circuit controls the first, second, and third switches so that if the first switch is disconnected, the second and third switch are controlled by the local processor.

23. The circuit board of claim 18, wherein the two wire serial bus is a two wire serial bus.

24. The circuit board of claim 18, wherein at least one of a voltage monitor and a temperature sensor are connected to the second portion of the two wire serial bus.

25. The circuit board of claim 18, wherein an ID EPROM is connected to the third portion of the two wire serial bus.